REMARKS

Claim Disposition

Claims 1 – 12 are pending in the present application. Claims 2 – 4 have been objected to. Claims 1 and 5 – 12 have been rejected. Claim 9 has been amended to more particularly point out and distinctly claim that which Applicant claims as his invention. Claim 9 has also been amended to depend from claim 7 and provide correct antecedent basis. According to the Examiner's suggestion, Claim 2 has been rewritten in independent form including all of the limitations of the base claim and any intervening claims.

No new matter has been introduced by these amendments. Support for the amendments may readily be found throughout the specification. Reconsideration and allowance of the claims is respectfully requested in view of the above amendments and the following remarks.

Claim Objections

Claims 2 - 4 have been objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Applicant appreciates the Examiner's indication of the allow ability of claims 2 – 4. Claim 2 has been rewritten in independent form. Claims 2-4 should now be allowable. Claim 9 has been objected to as including informalities. Applicant appreciates the Examiner's observations and has amended claim 9 to address the Examiner's concerns.

Claim Rejections Under 35 U.S.C. § 103

Claims 1 and 5 - 12 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Rosefield et al., U.S. Patent No. 6,541,996, hereinafter referred to as Rosefield; in view of Yoshizaki, U.S. Patent No. 6,400,177, hereinafter referred to as Yoshizaki. Applicant respectfully traverses. Rosefield is cited in the Office Action as allegedly disclosing:

> "a method (see Figs 1-4) for measuring the impedance of driver devices (102, IMPEDANCE MEASUREMENT) during a test (see Fig. 2, pull up test EN and pull down test EN) being carried out before the regular operation of the semiconductor device (chip), the driver device (102 of the semiconductor device including each a pull-up circuit (204, pull up impedance matching array) and a pull-down circuit (206, pull down impedance matching array) (Col. 2, lines 54 – 65 'on-chip programmable pull up impedance matching array", the method comprising:"
>
> "joint activating of both the pull-up circuit (see Fig. 3, step 301 enable pull up imped array) and the pull-down circuit (see Fig 3, step 308 enable pull down imped array), and"
>
> "determining a total impedance of he pull up and pull down circuits (see Col. 9, lines 21-22 and 27-29)."

It is acknowledged in the Final Office Action that Rosefield "does not disclose the step of determining a first current flowing through the pull-up circuit or the pull-down circuit."

Yoshizaki is cited in the Final Office Action for allegedly disclosing:

> "an output driver (see Fig. 4) comprising a pull-up circuit (P1-4) and a pull-down circuit (N1-4). Yoshizaki exclusively teaches a method for meeting specified output impedance and current characteristics comprising the step of determining a first current flow (ILH,IHL) through a pull-down circuit (P1-4) or pull down circuit (N1-4) (see Col. 4, lines 15 - 65)".

It is suggested in the Final Office Action that it would have been obvious to incorporate the step of determining the current flow through the pull-down circuit as taught by Yoshizaki into Rosefield.

The Examiner further states:

> "With respect to claims 5-6, Yoshizaki ('177) discloses determining a voltage dropping over the pull-up and/or pull-down circuit, in particular with jointly activated pull-up and pull-down circuits (see Col. 4, lines 17-48)."
>
> "With respect to claim 7, Yoshizaki ('177) discloses that the method steps are performed several times in sequence (see Fig. 3, step 314 "wait for restart"), each with different settings of transistors contained in the pull-up or pull down circuit (see Fig. 4 transistors contained in the pull up circuit (204) and in the pull down circuit (206))."

> "With respect to claim 9, Yoshizaki ('177) discloses that on the basis of the first current and voltage dropping over the pull up and pull down circuits as determined (see Col. 4, lines 17-48), the "setting" is elected (see Col. 3, line 16 "to set an impedance lever") that is to be used during regular operation of the device."
>
> "With respect to claim 11, Rosefield et al ('996) discloses that a test device (comparator 209) is a test device not used for the driving of output signals during the regular operation of the semiconductor device and is for selecting the driver setting for at least one other semiconductor device (chip) during the test carried out before the regular operation of the at least one other semiconductor device (chip)."
>
> "With respect to claim 12, Rosefield et al ('996) discloses that the test device (comparator 209) is connected with a device (208) provided on the semiconductor device (chip) itself, by means of which a voltage dropping over the pull-up and/or pull-down circuit is determined."

For an obviousness rejection to be proper, the Examiner must meet the burden of establishing a *prima facie* case of obviousness. *In re Fine*, U.S.P.Q.2d 1596, 1598 (Fed. Cir.1988). The Examiner must meet the burden of establishing that all elements of the invention are disclosed in the prior art; that the prior art relied upon, coupled with knowledge generally available in the art at the time of the invention, must contain some suggestion or incentive that would have motivated the skilled artisan to modify a reference or combined references; and that the proposed modification of the prior art must have had a reasonable expectation of success, determined from the vantage point of the skilled artisan at the time the invention was made. *In re Fine*, 5 U.S.P.Q.2d 1596, 1598 (Fed. Cir. 1988); *In re Wilson*, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970); *Amgen v. Chugai Pharmaceuticals Co.*, 927 U.S.P.Q.2d, 1016, 1023 (Fed. Cir.1996).

Applicant respectfully contends that neither Rosefield nor Yoshizaki, whether alone, or in combination, teaches or discloses each element of the invention. Applicant respectfully disagrees with the Examiner's suggested interpretation that the combination of Rosefield and Yoshizaki suggests a method for measuring and trimming the impedance of a driver device in a semiconductor device during a test being carried out before the regular operation of the semiconductor device, with joint activating of both the pull-up circuit and

pull-down circuit; and determining a first current flowing through the pull-up circuit or the pull-down circuit, respectively, with jointly activated pull-up and pull-down circuits during the test carried out before the regular operation of the semiconductor device.

In particular, the Examiner suggests that Rosefield teaches jointly activating the pull-up and pull-down circuits, to support the rejection, the Examiner refers to Figure 3, step 301 and Fig. 3 step 308. However, Figure 3 includes no teaching or disclosure whatsoever that would suggest jointly activating the pull-up and pull-down circuits. In fact, Fig. 3 clearly shows that step 308 is subsequent to step 301. That is, the operation of the pull-down impedance array is conducted *subsequent* to the operation and measurement for the pull-up impedance array. This interpretation is made more evident by referral to the description in the specification at Col. 7, line 62 to Col. 8 line 24. The teachings of Rosefield clearly indicate determining suitable impedance for the pull-up impedance matching array, and then the same function for the pull-down impedance matching array. Rosefield also states, following the evaluation for the pull-up impedance matching array: "Similar to the operation with respect to ... pull-up impedance matching array ... this is continued until ... the pull down matching array is matched. Furthermore, Rosefield with reference to Figure 5 and the alternative embodiment directed to configuring the pull-down array, Rosefield states: "**Subsequently** (emphasis added), the same impedance setting ... is used to configure the pull-up impedance matching array".

Finally, reference to Claim 1 makes it most evident that Rosefield clearly teaches a sequential operation of the pull-up impedance matching array and the pull-down impedance matching array. Claim 1 clearly states at line 11 (Col 9, line 28) "*subsequently* determining a second impedance adjustment level..." The claims of Rosefield clearly provide the evidence that Rosefield provides for subsequent operation of the pull-up impedance matching array and pull-down impedance matching array. Therefore, because Rosefield does not disclose or teach, "jointly activated pull-up and pull-down circuits" as suggested in the Final Office Action, it cannot render Applicant's claim 1 unpatentable. Thus Claim 1 is allowable; the rejection is improper and should be withdrawn.

Furthermore, as acknowledged in the Final Office Action, Rosefield does not disclose the step of **determining a first current flowing through the pull-up or the pull-**

down circuit, respectively with jointly activated pull-up and pull-down circuits. To support the rejection, the Examiner has referred to Yoshizaki at Figure 4, and Col. 4, lines 15 – 65 as allegedly disclosing the claimed element. However, Yoshizaki does not teach or disclose **determining a first current** ... **with jointly activated** pull-up and pull down circuits as the Examiner suggest. Yoshizaki at Column 4, lines 1-5 specifically teaches complementary operation of the pull up and pull down transistors therein. Hence, Yoshizaki does not teach or suggest determining a first current flowing through the pull-up circuit or the pull-down circuit, respectively, with **jointly activated** pull-up and pull-down circuits during a test carried out before a regular operation of the semiconductor device, as the Applicant has claimed. Therefore, because Yoshizaki does not teach or disclose an element of Applicant's claims it cannot render the Applicant's claim unpatentable. Thus Claim 1 is allowable, the rejection is improper and should be withdrawn.

In conclusion, neither Rosefield nor Yoshizaki, whether alone or in combination teaches or discloses numerous elements of the claims. Therefore, Rosefield or Yoshizaki, whether alone or in combination cannot render Applicant's claims unpatentable. Thus, Claim 1 is patentable; the rejection is improper and should be withdrawn.

In view of the above discussion, Claims 2 - 12 depend from Claim 1, and include all of the corresponding limitations thereof. Claim 1 is not taught by Rosefield or Yoshizaki, whether alone or in combination, therefore, Claims 2 - 12 cannot be taught by Rosefield or Yoshizaki either. Thus, Claims 2 – 12 are allowable; the rejections are improper and they should be withdrawn.

The amendments and arguments presented herein are made for the purposes of better defining the invention, rather than to overcome the rejections for patentability. The claims have not been amended to overcome the prior art and therefore, no presumption should attach that either the claims have been narrowed over those earlier presented, or that subject matter or equivalents thereof to which the Applicant is entitled has been surrendered.

CONCLUSION

It is believed that the foregoing remarks are fully responsive to the Office Action and that the claims herein should be allowable to the Applicant. Accordingly, reconsideration and allowance of Claims 1 – 12 are respectfully requested. In the event the Examiner has any queries regarding the instantly submitted response, the undersigned respectfully requests the courtesy of a telephone conference to discuss any matters in need of attention.

Respectfully submitted,

ARENDT & ASSOCIATES
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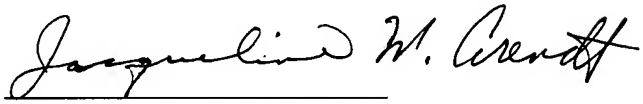
By 

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